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EXAMINER	
LAFORGIA, CHRISTIAN A	
ART UNIT	PAPER NUMBER
2155	3

DATE MAILED: 05/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/591,080	GINSBERG ET AL.	
	Examiner	Art Unit	
	Christian La Forgia	2155	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☒ Claim(s) *32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☒ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Requirements for Information – 37 CFR § 1.105

1. Applicant and the assignee of this application are required under 37 CFR 1.105 to provide the following information that the examiner has determined is reasonably necessary to the examination of this application.

2. In response to this requirement, please provide the names of any products or services that have incorporated the claimed subject matter, especially the technical disclosures, user guides, and/or white papers of the following products as found on the Applicant's website from 25 April 1999 (found via http://www.archive.org): the IXIA 200 Traffic Generator and Analyzer, the IXIA 1600, IxExplorer, the IXIA LM1000T, the IXIA LM1000LX, the IXIA LM1000SX, and the IXIA LM1000GBIC.

3. In responding to those requirements that require copies of documents, where the document is a bound text or a single article over 50 pages, the requirement may be met by providing copies of those pages that provide the particular subject matter indicated in the requirement, or where such subject matter is not indicated, the subject matter found in applicant's disclosure.

4. The fee and certification requirements of 37 CFR 1.97 are waived for those documents submitted in reply to this requirement. This waiver extends only to those documents within the scope of this requirement under 37 CFR 1.105 that are included in the applicant's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this requirement and any information disclosures beyond the scope of this requirement under 37 CFR 1.105 are subject to the fee and certification requirements of 37 CFR 1.97.

5. The applicant is reminded that the reply to this requirement must be made with candor and good faith under 37 CFR 1.56. Where the applicant does not have or cannot readily obtain an item of required information, a statement that the item is unknown or cannot be readily obtained will be accepted as a complete reply to the requirement for that item.

6. This requirement is an attachment of the enclosed Office action. A complete reply to the enclosed Office action must include a complete reply to this requirement. The time period for reply to this requirement coincides with the time period for reply to the enclosed Office action.

AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

1. Claims 1 through 37 are presented for examination.

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

3. The oath or declaration is defective because:

> It does not identify the mailing or post office address of each inventor. A mailing or post office address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing or post office address should include the ZIP Code designation. The mailing or post office address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.

Drawings

4. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings.

5. The Patent and Trademark Office no longer makes drawing changes. See 1017 O.G. 4. It is applicant's responsibility to ensure that the drawings are corrected. Corrections must be made in accordance with the instructions below.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities -- 37 CFR 1.85

> New corrected drawings must be filed with the changes incorporated therein. Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the "Notice of Allowability."

Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136 for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

2. **Corrections other than Informalities Noted by Draftsperson on form PTO-948.**

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Timing of Corrections

Applicant is required to submit acceptable corrected drawings within the time period set in the Office action. See 37 CFR 1.185(a). Failure to take corrective action within the set (or extended) period will result in **ABANDONMENT** of the application.

Specification

6. The abstract of the disclosure is objected to because it is more than 150 words.

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1 through 33, 35, and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent No. 6,321,264 to Fletcher et al., (hereinafter Fletcher).

9. As per claim 1, Fletcher teaches a method of determining a time delay for a round-trip transmission of data comprising:

10. receiving a first data packet comprising a first IP source address, a first IP destination address, a first TCP source port, a first TCP destination port, and a first time stamp indicating a first time when the first data packet was transmitted (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 12, lines 24-47; column 13, lines 7-14; column 14, lines 27-45);

11. inserting the first IP destination address as a second IP source address in a second data packet (Figures 3 [blocks 390, 395], 5 [block 525, 530]; column 8, lines 15-37; column 9, lines 25-37; column 10, lines 57-64; column 12, lines 47-65);

12. inserting the first IP source address as a second IP destination address in the second data packet (Figures 3 [blocks 390, 395], 5 [block 525, 530]; column 8, lines 15-37; column 9, lines 25-37; column 10, lines 57-64; column 12, lines 47-65);

13. inserting the first TCP destination port as a second TCP source port in the second data packet (Figures 3 [blocks 390, 395], 5 [block 525, 530]; column 8, lines 15-37; column 9, lines 25-37; column 10, lines 57-64; column 12, lines 47-65);

14. inserting the first TCP source port as a second TCP destination port in the second data packet (Figures 3 [blocks 390, 395], 5 [block 525, 530]; column 8, lines 15-37; column 9, lines 25-37; column 10, lines 57-64; column 12, lines 47-65);

15. inserting the first time stamp as a second time stamp in the second data packet (Figures 3 [blocks 390, 395], 5 [block 525, 530]; column 8, lines 15-37; column 9, lines 25-37; column 10, lines 57-64; column 12, lines 47-65); and

16. transmitting the second data packet (Figures 3 [blocks 390, 395], 5 [block 525, 530]; column 8, lines 15-37; column 9, lines 25-37; column 10, lines 57-64; column 12, lines 47-65).

17. Regarding claim 2, Fletcher teaches further comprising:

18. transmitting the first data packet at the first time (column 8, lines 1-63);

19. receiving the second data packet at a second time (column 8, lines 1-63); and

20. determining a difference between the first time in the second time stamp and the second time to establish the time delay for the round-trip transmission of data (column 8, lines 1-63).

21. Regarding claim 3, Fletcher teaches further comprising:

22. validating the first IP destination address while receiving the first data packet, before inserting the first IP destination address, before inserting the first IP source address, before inserting the first TCP destination port, before inserting the first TCP source port, and before transmitting the second data packet (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 11, lines 20-32); and

23. validating the first TCP destination port while receiving the first data packet, before inserting the first IP destination address, before inserting the first IP source address, before inserting the first TCP destination port, before inserting the first TCP source port, and before transmitting the second data packet (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 11, lines 20-32).

24. Regarding claim 4, Fletcher teaches wherein:

25. inserting the first IP destination address occurs while transmitting the second data packet (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65); and

26. inserting the first IP source address occurs while transmitting the second data packet (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65).

27. Regarding claim 5, Fletcher teaches wherein:

28. inserting the first TCP destination port occurs while transmitting the second data packet (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65); and

29. inserting the first TCP source port occurs while transmitting the second data packet (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65).

30. Regarding claim 6, Fletcher teaches wherein:

31. inserting the first time stamp occurs while transmitting the second data packet (column 8, lines 1-63).

32. Regarding claim 7, Fletcher teaches further comprising:

33. providing the first data packet to further comprise a first IP checksum, a first TCP checksum, and a first CRC checksum (column 10, lines 57-64; column 11, lines 48-65);

34. validating the first IP checksum while receiving the first data packet (column 10, lines 57-64; column 11, lines 48-65);

35. validating the first TCP checksum while receiving the first data packet (column 10, lines 57-64; column 11, lines 48-65); and

36. validating the first CRC checksum (column 10, lines 57-64; column 11, lines 48-65).

The Examiner believes that the validating of the checksum is inherently included in the invention of Fletcher, and for a better understanding has enclosed Chapters 7 and 13 of ***Internetworking with TCP/IP Principles, Protocols, and Procedures*** by Douglas E. Comer, which provide a more in depth analysis of the TCP and IP headers.

37. With regards to claim 8, Fletcher teaches further comprising:

38. storing the first IP source address and the first IP destination address before validating the first IP checksum (Figures 3 [blocks 390, 395], 5 [block 525, 530]; column 8, lines 15-37; column 9, lines 25-37; column 10, lines 57-64; column 11, lines 48-65; column 12, lines 47-65); and

39. storing the first TCP source port and the first TCP destination port after validating the first IP checksum and before validating the first TCP checksum (Figures 3 [blocks 390, 395], 5 [block 525, 530]; column 8, lines 15-37; column 9, lines 25-37; column 11, lines 48-65; column 10, lines 57-64; column 12, lines 47-65). The Examiner believes that the validating of the

checksum is inherently included in the invention of Fletcher, and for a better understanding has enclosed Chapters 7 and 13 of ***Internetworking with TCP/IP Principles, Protocols, and Procedures*** by Douglas E. Comer, which provide a more in depth analysis of the TCP and IP headers.

40. With regards to claim 9, Fletcher teaches wherein:

41. validating the first TCP checksum occurs after validating the first IP checksum and before validating the first CRC checksum. The Examiner believes that the checking of the header checksums is inherent, and has enclosed Chapters 7 and 32 of ***Internetworking with TCP/IP Principles, Protocols, and Procedures*** by Douglas E. Comer, specifically pages 586 to 587, which provide a more in depth analysis of encapsulation.

42. With regards to claim 10, Fletcher teaches wherein:

43. validating the first CRC checksum occurs after receiving the first data packet (column 10, lines 57-64; column 11, lines 48-65). The Examiner believes that the validating of the checksum is inherently included in the invention of Fletcher, and for a better understanding has enclosed Chapters 7 and 13 of ***Internetworking with TCP/IP Principles, Protocols, and Procedures*** by Douglas E. Comer, which provide a more in depth analysis of the TCP and IP headers.

44. With regards to claim 11, Fletcher teaches further comprising:

45. determining a second IP checksum for the second data packet (column 10, lines 57-64; column 11, lines 48-65);

46. inserting the second IP checksum into the second data packet while transmitting the second data packet (column 10, lines 57-64; column 11, lines 48-65);

47. determining a second TCP checksum for the second data packet (column 10, lines 57-64; column 11, lines 48-65); and

48. inserting the second TCP checksum into the second data packet while transmitting the second data packet (column 10, lines 57-64; column 11, lines 48-65). The Examiner believes that the validating of the checksum is inherently included in the invention of Fletcher, and for a better understanding has enclosed Chapters 7 and 13 of ***Internetworking with TCP/IP Principles, Protocols, and Procedures*** by Douglas E. Comer, which provide a more in depth analysis of the TCP and IP headers.

49. Regarding claim 12, Fletcher teaches wherein:

50. inserting the first IP destination address occurs while transmitting the second data packet (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

51. inserting the first IP source address occurs while transmitting the second data packet (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

52. inserting the first TCP destination port occurs while transmitting the second data packet (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

53. inserting the first TCP source port occurs while transmitting the second data packet (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65); and

54. inserting the first time stamp occurs while transmitting the second data packet (column 8, lines 1-63).

55. Regarding claim 13, Fletcher teaches wherein:

56. inserting the first IP destination address occurs after inserting the second IP checksum (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

57. inserting the first IP source address occurs after inserting the first IP destination address (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

58. inserting the first TCP destination port occurs after inserting the first IP source address (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65); and

59. inserting the first TCP source port occurs after inserting the first TCP destination port and before inserting the second TCP checksum (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65).

60. Regarding claim 14, Fletcher teaches further comprising:

61. providing the first data packet to further comprise a first data pattern (Figures 5, 7, & 8; column 9, lines 25-57; column 10, lines 1-56; column 12, lines 1-23); and

62. inserting a second data pattern into the second data packet (Figures 5, 7, & 8; column 9, lines 25-57; column 10, lines 1-56; column 12, lines 1-23).

63. Regarding claim 15, Fletcher teaches wherein:

64. inserting the second data pattern occurs while transmitting the second data packet (Figures 5, 7, & 8; column 9, lines 25-57; column 10, lines 1-56; column 12, lines 1-23).

65. Regarding claim 16, Fletcher teaches further comprising:

66. providing the first data packet to further comprise a first TCP flag (column 10, lines 57-64); and

67. inserting the first TCP flag as a second TCP flag into the second data packet (column 10, lines 57-64). The Examiner believes that the inserting of the TCP flag is inherently included in the invention of Fletcher, and for a better understanding has enclosed Chapter 13, specifically pages 221 through 222, of ***Internetworking with TCP/IP Principles, Protocols, and Procedures*** by Douglas E. Comer, which provide a more in depth analysis of the TCP flags.

68. Regarding claim 17, Fletcher teaches further comprising:

69. validating the first TCP flag while receiving the first data packet, before inserting the first IP destination address, before inserting the first IP source address, before inserting the first TCP destination port, before inserting the first TCP source port, before transmitting the second data packet, and before inserting the first TCP flag (column 10, lines 57-64; column 11, lines 48-65). The Examiner believes that the validating of the TCP flag is inherently included in the invention of Fletcher, and for a better understanding has enclosed Chapter 13, specifically pages 221 through 222, of ***Internetworking with TCP/IP Principles, Protocols, and Procedures*** by Douglas E. Comer, which provide a more in depth analysis of the TCP flags.

70. Regarding claim 18, Fletcher teaches wherein:

71. inserting the second TCP flag occurs while transmitting the second data packet (Figures 5, 7, & 8; column 9, lines 25-57; column 10, lines 1-56; column 12, lines 1-23). The Examiner believes that the validating of the TCP flag is inherently included in the invention of Fletcher, and for a better understanding has enclosed Chapter 13, specifically pages 221 through 222, of ***Internetworking with TCP/IP Principles, Protocols, and Procedures*** by Douglas E. Comer, which provide a more in depth analysis of the TCP flags.

72. Regarding claim 19, Fletcher teaches further comprising:

73. providing the first data packet to further comprise two TCP flags (column 10, lines 57-64; column 11, lines 48-65);

74. inserting the two TCP flags into the second data packet (column 10, lines 57-64; column 11, lines 48-65);

75. inserting an additional TCP flag into the second data packet, the additional TCP flag having a value of one (column 10, lines 57-64; column 11, lines 48-65); and

76. inserting three additional TCP flags into the second data packet, the three additional TCP flags each having a value of zero (column 10, lines 57-64; column 11, lines 48-65). The Examiner believes that the TCP flags are inherently included in the invention of Fletcher, and for a better understanding has enclosed Chapter 13, specifically pages 221 through 222, of ***Internetworking with TCP/IP Principles, Protocols, and Procedures*** by Douglas E. Comer, which provide a more in depth discussion of the TCP flags.

77. Regarding claim 20, Fletcher teaches further comprising:

78. providing the first data packet to further comprising six TCP flags (column 10, lines 57-64; column 11, lines 48-65);

79. inserting two of the six TCP flags into the second data packet (column 10, lines 57-64; column 11, lines 48-65);

80. inserting an additional TCP flag into the second data packet, the additional TCP flag having a value of one (column 10, lines 57-64; column 11, lines 48-65); and

81. inserting three additional TCP flags into the second data packet, the three additional TCP flags each having a value of zero (column 10, lines 57-64; column 11, lines 48-65). The Examiner believes that the TCP flags are inherently included in the invention of Fletcher, and for a better understanding has enclosed Chapter 13, specifically pages 221 through 222, of ***Internetworking with TCP/IP Principles, Protocols, and Procedures*** by Douglas E. Comer, which provide a more in depth discussion of the TCP flags.

82. With regards to claim 21, Fletcher teaches further comprising:

83. providing a FIN flag and a SYN flag for the two of the six TCP flags (column 10, lines 57-64; column 11, lines 48-65); and

84. providing an ACK flag for the additional TCP flag (column 10, lines 57-64; column 11, lines 48-65). The Examiner believes that the TCP flags are inherently included in the invention of Fletcher, and for a better understanding has enclosed Chapter 13, specifically pages 221 through 222, of ***Internetworking with TCP/IP Principles, Protocols, and Procedures*** by Douglas E. Comer, which provide a more in depth discussion of the TCP flags.

85. Regarding claim 22, Fletcher teaches further comprising:

86. providing the first data packet to further comprise a first IP checksum, first TCP flags, a first TCP checksum, and a first CRC checksum (column 10, lines 57-64; column 11, lines 48-65);

87. validating the first IP checksum while receiving the first data packet (column 10, lines 57-64; column 11, lines 48-65);

88. validating the first TCP checksum while receiving the first data packet (column 10, lines 57-64; column 11, lines 48-65);

89. validating the first CRC checksum after receiving the first data packet (column 10, lines 57-64; column 11, lines 48-65);

90. determining a second IP checksum for the second data packet (column 10, lines 57-64; column 11, lines 48-65);

91. inserting and the second IP checksum into the second data packet while transmitting the second data packet (column 10, lines 57-64; column 11, lines 48-65);

92. inserting the first TCP flags as second TCP flags into the second data packet while transmitting the second data packet (column 10, lines 57-64; column 11, lines 48-65);

93. determining a second TCP checksum for the second data packet (column 10, lines 57-64; column 11, lines 48-65);

94. inserting the second TCP checksum into the second data packet while transmitting the second data packet (column 10, lines 57-64; column 11, lines 48-65);

95. determining a second CRC checksum for the second data packet (column 10, lines 57-64; column 11, lines 48-65); and

96. inserting the second CRC checksum into the second data packet while transmitting the second data packet (column 10, lines 57-64; column 11, lines 48-65). The Examiner believes that the validating of the checksum and the TCP flags are inherently included in the invention of Fletcher, and for a better understanding has enclosed Chapters 7 and 13 of ***Internetworking with TCP/IP Principles, Protocols, and Procedures*** by Douglas E. Comer, which provide a more in depth analysis of the TCP and IP headers.

97. Concerning claim 23, Fletcher teaches wherein:

98. inserting the first IP destination address occurs while transmitting the second data packet (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

99. inserting the first IP source address occurs while transmitting the second data packet (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

100. inserting the first TCP destination port occurs while transmitting the second data packet (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

101. inserting the first TCP source port occurs while transmitting the second data packet (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65); and

102. inserting the first time stamp occurs while transmitting the second data packet (column 8, lines 1-63).

103. With regards to claim 24, Fletcher teaches wherein:

104. inserting the first IP destination address occurs after inserting the second IP checksum (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

105. inserting the first IP source address occurs after inserting the first IP destination address (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

106. inserting the first TCP destination port occurs after inserting the first IP source address (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

107. inserting the first TCP source port occurs after inserting the first TCP destination port (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

108. inserting the first TCP flags occurs after inserting the first TCP source port (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

109. inserting the second TCP checksum occurs after inserting the first TCP flags (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

110. inserting the first time stamp occur after inserting the second TCP checksum (column 8, lines 1-63); and

111. inserting the second CRC checksum occurs after inserting the first time stamp (column 8, lines 1-63).

112. With regards to claim 25, Fletcher teaches further comprising:

113. providing the first data packet to further comprise a first data pattern (Figures 5, 7, & 8; column 9, lines 25-57; column 10, lines 1-56; column 12, lines 1-23); and

114. inserting a second data pattern into the second data packet while transmitting the second data packet (Figures 5, 7, & 8; column 9, lines 25-57; column 10, lines 1-56; column 12, lines 1-23).

115. With regards to claim 26, Fletcher teaches further comprising:

116. transmitting the first data packet at the first time from a first electronic apparatus having the first IP source address and the first TCP source port (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 12, lines 24-47; column 13, lines 7-14; column 14, lines 27-45);

117. receiving the second data packet at a second time and at the first electronic apparatus having the second IP destination address and the second TCP destination port (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 12, lines 24-47; column 13, lines 7-14; column 14, lines 27-45); and

118. subtracting the first time in the second time stamp from the second time to determine the time delay for the round-trip transmission of data (column 8, lines 1-63), wherein:

119. receiving the first data packet further comprises receiving the first data packet at a second electronic apparatus having the first IP destination address and the first TCP destination port (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 12, lines 24-47; column 13, lines 7-14; column 14, lines 27-45); and

120. transmitting the second data packet further comprises transmitting the second data packet from the second electronic apparatus having the second IP source address and the second TCP source port (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 12, lines 24-47; column 13, lines 7-14; column 14, lines 27-45).

121. With regards to claim 27, Fletcher teaches wherein:

122. inserting the first IP destination address occurs after inserting the second IP checksum (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

123. inserting the first IP source address occurs after inserting the first IP destination address (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

124. inserting the first TCP destination port occurs after inserting the first IP source address (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

125. inserting the first TCP source port occurs after inserting the first TCP destination port (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

126. inserting the first TCP flags occurs after inserting the first TCP source port (Figures 7 [block 730], 8 [block 863]; column 10, lines 57-64; column 12, lines 48-65);

127. inserting the second TCP checksum occurs after inserting the first TCP flags (column 8, lines 1-63);

128. inserting the first time stamp occur after inserting the second TCP checksum (column 8, lines 1-63); and

129. inserting the second CRC checksum occurs after inserting the first time stamp (column 8, lines 1-63).

130. With regards to claim 28, Fletcher teaches further comprising:

131. providing the first data packet to further comprise a first data pattern (Figures 5, 7, & 8; column 9, lines 25-57; column 10, lines 1-56; column 12, lines 1-23); and

132. inserting a second data pattern into the second data packet while transmitting the second data packet (Figures 5, 7, & 8; column 9, lines 25-57; column 10, lines 1-56; column 12, lines 1-23).

133. With regards to claim 29, Fletcher teaches further comprising:

134. transmitting the first data packet at the first time from a first electronic apparatus having the first IP source address and the first TCP source port (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 12, lines 24-47; column 13, lines 7-14; column 14, lines 27-45);

135. receiving the second data packet at a second time and at the first electronic apparatus having the second IP destination address and the second TCP destination port (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 12, lines 24-47; column 13, lines 7-14; column 14, lines 27-45); and

136. subtracting the first time in the second time stamp from the second time to determine the time delay for the round-trip transmission of data (column 8, lines 1-63), wherein:

137. receiving the first data packet further comprises receiving the first data packet at a second electronic apparatus having the first IP destination address and the first TCP destination port (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 12, lines 24-47; column 13, lines 7-14; column 14, lines 27-45); and

138. transmitting the second data packet further comprises transmitting the second data packet from the second electronic apparatus having the second IP source address and the second TCP

source port (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 12, lines 24-47; column 13, lines 7-14; column 14, lines 27-45).

139. Regarding claim 30, Fletcher teaches further comprising:

140. waiting for the first data packet (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 12, lines 24-47; column 13, lines 7-14; column 14, lines 27-45);

141. checking a status of a first memory portion (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 11, lines 31-67).

142. storing a portion of the first data packet if the first memory portion is available, the portion of the first memory portion comprising the first IP source address, the first IP destination address, the first TCP source port, and the first TCP destination port (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 11, lines 31-67);

143. checking a validity of the first data packet (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 11, lines 31-67);

144. setting the status of the first memory portion to full if the first data packet is valid (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 11, lines 31-67);

145. checking a status of a second memory portion (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 11, lines 31-67);

146. transferring the portion of the first data packet from the first memory portion to the second memory portion if the second memory portion is available and if the first data packet is valid (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 11, lines 31-67);

147. setting the status of the second memory portion to full (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 11, lines 31-67); and

148. setting the status of the first memory portion to empty (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 11, lines 31-67).

149. As per claim 31, Fletcher teaches an electronic apparatus for determining a time delay for a round-trip transmission of data comprising:

150. a data reception portion (Figure 2 [block 208], 3 [blocks 330 and 380], 4 [blocks 320 and 370], 5 [block 540]; column 6, line 51 to column 7, line 7);

151. an input memory portion coupled to the data reception portion (Figure 2 [blocks 202, 203, & 204]; column 6, line 51 to column 7, line 7);

152. a data validity portion coupled to the data reception portion (Figure 2 [blocks 202, 203, & 204], 5 [block 525, 526, 540], 7, 8; column 6, line 51 to column 7, line 7; column 9, lines 13-67; column 10, lines 1-28);

153. a first memory and data transfer management portion coupled to the input memory portion and the data validity portion (Figure 2 [blocks 202, 203, & 204], 5 [block 525, 526, 540], 7, 8; column 6, line 51 to column 7, line 7; column 9, lines 13-67; column 10, lines 1-28);

154. a second memory and data transfer management portion coupled to the first memory and data transfer management portion (Figure 2 [blocks 202, 203, & 204]; column 6, line 51 to column 7, line 7);

155. an output memory portion coupled to the input memory portion and the second memory and data transfer management portion (Figure 2 [blocks 202, 203, & 204]; column 6, line 51 to column 7, line 7);

156. a data pattern management portion coupled to the second memory and data transfer management portion (Figures 5, 7, & 8; column 9, lines 25-57; column 10, lines 1-56; column 12, lines 1-23);

157. a header format portion coupled to the output memory portion (Figure 2 [block 208], 3 [blocks 330 and 380], 4 [blocks 320 and 370], 5 [block 540]; column 6, line 51 to column 7, line 7); and

158. a data transmission portion coupled to the header format portion and the data pattern management portion (Figure 2 [block 208], 3 [blocks 330 and 380], 4 [blocks 320 and 370], 5 [block 540]; column 6, line 51 to column 7, line 7).

159. With regards to claim 32, Fletcher teaches further comprising:

160. an incoming data portion comprising:

the data reception portion (Figure 2 [block 208], 3 [blocks 330 and 380], 4 [blocks 320 and 370], 5 [block 540]; column 6, line 51 to column 7, line 7);

the input memory portion (Figure 2 [blocks 202, 203, & 204]; column 6, line 51 to column 7, line 7);

the data validity portion (Figure 2 [blocks 202, 203, & 204], 5 [block 525, 526, 540], 7, 8; column 6, line 51 to column 7, line 7; column 9, lines 13-67; column 10, lines 1-28); and

the first memory and data transfer management portion (Figure 2 [blocks 202, 203, & 204], 5 [block 525, 526, 540], 7, 8; column 6, line 51 to column 7, line 7; column 9, lines 13-67; column 10, lines 1-28); and

161. an outgoing data portion comprising:

the second memory and data transfer management portion (Figure 2 [blocks 202, 203, & 204]; column 6, line 51 to column 7, line 7);

the output memory portion (Figure 2 [blocks 202, 203, & 204]; column 6, line 51 to column 7, line 7);

the data pattern management portion (Figures 5, 7, & 8; column 9, lines 25-57; column 10, lines 1-56; column 12, lines 1-23);

the header format portion (Figure 2 [block 208], 3 [blocks 330 and 380], 4 [blocks 320 and 370], 5 [block 540]; column 6, line 51 to column 7, line 7); and

the data transmission portion (Figure 2 [block 208], 3 [blocks 330 and 380], 4 [blocks 320 and 370], 5 [block 540]; column 6, line 51 to column 7, line 7).

162. With regards to claim 33, Fletcher teaches wherein:

163. the input memory portion stores a portion of an incoming data packet (Figure 2 [blocks 202, 203, & 204]; column 6, line 51 to column 7, line 7);

164. the first and second memory and data transfer management portions manage a transfer of the portion of the incoming data packet from the input memory portion to the output memory portion (Figure 2 [blocks 202, 203, & 204], 5 [block 525, 526, 540], 7, 8; column 6, line 51 to column 7, line 7; column 9, lines 13-67; column 10, lines 1-28);

165. the data validity portion validates the incoming data packet (Figures 5, 7, & 8; column 9, lines 25-57; column 10, lines 1-56; column 12, lines 1-23);

166. the output memory portion receives the portion of the incoming data packet from the input memory portion (Figure 2 [blocks 202, 203, & 204]; column 6, line 51 to column 7, line 7);

167. the data pattern management portion manages an insertion of a data pattern into an outgoing data packet (Figures 5, 7, & 8; column 9, lines 25-57; column 10, lines 1-56; column 12, lines 1-23); and

168. a header format portion inserts an IP source address, an IP destination address, a TCP source port, a TCP destination port, TCP flags, and a time stamp into the outgoing data packet (Figures 3 [blocks 390, 395], 5 [block 525], 7 [block 730]; column 8, lines 1-63; column 10, line 57-64; column 12, lines 24-47; column 13, lines 7-14; column 14, lines 27-45).

169. With regards to claim 35, Fletcher teaches further comprising:

170. a data pattern memory portion coupling the data pattern management portion to the data transmission portion (Figures 5, 7, & 8; column 9, lines 25-57; column 10, lines 1-56; column 12, lines 1-23).

171. Regarding claim 36, Fletcher teaches wherein:

172. the data pattern memory portion is a dynamic random access memory (Figures 5, 7, & 8; column 9, lines 25-57; column 10, lines 1-56; column 12, lines 1-23).

Claim Rejections - 35 USC § 103

173. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

174. Claims 34 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fletcher in view of United States Patent No. 6,446,121 to Shah et al., (hereinafter Shah).

175. With regards to claim 34, Fletcher does not teach wherein:

176. the input memory portion, the output memory portion, the first and second memory and data transfer management portions, the data validity portion, the data reception portion, the data transmission portion, the header format portion, and the data pattern management portion are located within a field-programmable gate array.

177. Shah teaches wherein:

178. the input memory portion, the output memory portion, the first and second memory and data transfer management portions, the data validity portion, the data reception portion, the data transmission portion, the header format portion, and the data pattern management portion are located within a field-programmable gate array (column 5, lines 25-49). Therefore it would have been obvious at the time the invention was made to incorporate the system of Fletcher on the

field programmable gate array of Shah, it would inevitably save CPU time and thus make the system more efficient. One would be motivated to include the field-programmable gate array of Shah because it would allow the system to calculate the round trip time to every device on the network, and from there determine the best route or path. See Shah, column 3, lines 22-34.

179. Concerning claim 37, Fletcher does not teach wherein:

180. the input memory portion, the output memory portion, the first and second memory and data transfer management portions, the data validity portion, the data reception portion, the data transmission portion, the header format portion, and the data pattern management portion are located within a field-programmable gate array.

181. Shah teaches wherein:

182. the input memory portion, the output memory portion, the first and second memory and data transfer management portions, the data validity portion, the data reception portion, the data transmission portion, the header format portion, and the data pattern management portion are located within a field-programmable gate array (column 5, lines 25-49). It would have been obvious at the time the invention was made to incorporate the system of Fletcher on the field programmable gate array of Shah, it would inevitably save CPU time and thus make the system more efficient. One would be motivated to include the field-programmable gate array of Shah because it would allow the system to calculate the round trip time to every device on the network, and from there determine the best route or path. See Shah, column 3, lines 22-34.

Claim Objections

183. Claim 32 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Conclusion

184. This Office action has an attached requirement for information under 37 CFR 1.105. A complete reply to this Office action must include a complete reply to the attached requirement for information. The time period for reply to the attached requirement coincides with the time period for reply to this Office action.

185. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

186. The following patents are cited to further show the state of the art with respect to round trip delay measurements, such as:

United States Patent No. 6,545,979 to Poulin, which is cited to show to show a round trip delay measurement method and device.

United States Patent No. 5,477,531 to McKee et al., which is cited to show a method and apparatus for testing a packet-based network.

United States Patent No. 5,450,394 to Gruber et al., which is cited to show a method and device for monitoring a delay in a telecommunications network.

United States Patent No. 6,222,825 to Mangin et al., which is cited to show an arrangement for determining link latency in a full-duplex network.

187. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian La Forgia whose telephone number is (703) 305-7704. The examiner can normally be reached on Monday thru Thursday 7-5.

188. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (703) 305-9648. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7240 for regular communications and (703) 746-7239 for After Final communications.

189. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Christian LaForgia
Patent Examiner
Art Unit 2155

clf
May 3, 2003

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